Customer No.: 31561
Docket No.: 13300-US-PA
Application No.: 10/711,667

AMENDMENTS

In The Claims:

1. (canceled)

2. (canceled)

3. (currently amended) A method of measuring at least two capacitor pairs, wherein each of the capacitor pairs comprises at least a first capacitor and a second capacitor, the method comprising:

providing a first switch to each ~~of the~~ capacitor pair respectively, each first switch having a first terminal and a second terminal, wherein [[a]]the first terminal of each ~~of the~~ first switch is connected to a terminal of the first capacitor of the corresponding capacitor pair, and ~~another~~ the second terminal of each ~~of the~~ first switch is connected to a first pad respectively;

providing a second switch to each ~~of the~~ capacitor pair respectively, each second switch having a first terminal and a second terminal, wherein [[a]]the first terminal of each ~~of the~~ second switch is connected to a terminal of the second capacitor of the corresponding capacitor pair, and ~~another~~ the second terminal of each ~~of the~~ second switch is connected to a second pad respectively;

providing a third switch to each ~~of the~~ capacitor pair respectively, each third switch having a first terminal and a second terminal, wherein [[a]]the first terminal of each ~~of the~~ third switch is connected to another terminal of the first capacitor and another terminal of the second capacitor of the corresponding capacitor pair; and

providing a P-type transistor, the P-type transistor having a gate, a drain and

source, wherein [[a]]the gate of the P-type transistor is connected to ~~another~~ the second terminal of [[the]]each third switch ~~of all of the capacitor pairs~~, the drain of the P-type transistor is connected to a third pad, and the source of the P-type transistor is connected to a fourth pad;

wherein a capacitance of one of the first capacitors, a capacitance of one of the second capacitors, or a ratio of a difference between the capacitance of the one of the first capacitors and the capacitance of the one of the second capacitors is measured via the first pad, the second pad, ~~and a source and a drain of the P-type transistor~~ the third pad and the fourth pad.

4. (currently amended) The method of claim 3, wherein when the first switch, the second switch and the third switch of one of the capacitor [[~~pair~~]]pairs are turned on, for the one of the capacitor [[~~pair~~]]pairs, the capacitance of the first capacitor thereof, the capacitance of the second capacitor thereof, or a ratio of a difference between the capacitance of the first capacitor and the capacitance of the second capacitor to an average of the capacitance of the first capacitor and the capacitance of the second capacitor thereof is measured via the first pad, the second pad, the third pad and the fourth pad.

5. (currently amended) The method of claim 3, wherein when the first switch and the third switch of one of the capacitor [[~~pair~~]]pairs, and the second switch and the third switch of another one of the capacitor [[~~pair~~]]pairs are turned on, the capacitance of the first capacitor of the one of the capacitor [[~~pair~~]]pairs, the capacitance of the second capacitor of the another one of the capacitor [[~~pair~~]]pairs, or a ratio of a difference

between the capacitance of the first capacitor of the one of the capacitor [[~~pair~~]]pairs and the capacitance of the second capacitor of the another one of the capacitor [[~~pair~~]]pairs to an average of the capacitance of the first capacitor of the one of the capacitor [[~~pair~~]]pairs and the capacitance of the second capacitor of the another one of the capacitor [[~~pair~~]]pairs is measured via the first pad, the second pad, the third pad and fourth pad.

6. (original) The method of claim 3, further comprising:

providing a selection circuit, connected to all of the first switches, the second switches and the third switches to selectively turn on or turn off the first switches, the second switches or the third switches.

7. (original) The method of claim 6, further comprising a step of automatically operating the method via the selection circuit.

8. (original) The method of claim 6, wherein the selection circuit comprises a shift register.

9. (currently amended) A circuit for measuring at least two capacitor pairs, wherein each of the capacitor pairs comprises at least a first capacitor and a second capacitor, the circuit comprising:

a plurality of first switches, each first switch having a first terminal and a second terminal, wherein [[a]]the first terminal of each ~~of the~~ first switch is connected to a terminal of the first capacitor of each of the capacitor pairs, and ~~another~~ the second terminal of ~~all of the~~ each first switch is connected to a first pad;

a plurality of second switches, each second switch having a first terminal and a second terminal, wherein [[a]]the first terminal of each ~~of the~~ second switch is connected

to a terminal of the second capacitor of each of the capacitor pairs, and ~~another~~ the second terminal of ~~all of the~~ each second switch is connected to a second pad;

a plurality of third switches, each third switch having a first terminal and a second terminal, wherein [[a]]the first terminal of each ~~of the~~ third switch is connected to another terminal of the first capacitor and another terminal of the second capacitor of each of the capacitor pairs; and

a P-type transistor, having a gate, a drain and source, wherein [[a]]the gate of the P-type transistor is connected to ~~another~~ the second terminal of [[the]]each third switch ~~of all of the capacitor pairs~~, the drain of the P-type transistor is connected to a third pad, and the source of the P-type transistor is connected to a fourth pad;

wherein a capacitance of one of the first capacitors, a capacitance of one of the second capacitors, or a ratio of a difference between the capacitance of the one of the first capacitors and the capacitance of the one of the second capacitors to an average of the capacitance of the one of the first capacitors and the capacitance of the one of the second capacitors is measured via the first pad, the second pad, ~~and a source and a drain of the P type transistor~~ the third pad, and the fourth pad.

10. (currently amended) The circuit of claim 9, wherein when the first switch, the second switch and the third switch of one of the capacitor [[~~pair~~]]pairs are turned on, for the one of the capacitor [[~~pair~~]]pairs, the capacitance of the first capacitor thereof, the capacitance of the second capacitor thereof, or a ratio of a difference between the capacitance of the first capacitor and the capacitance of the second capacitor to an average of the capacitance of the first capacitor and the capacitance of the second capacitor thereof is measured.

11. (currently amended) The circuit of claim 9, wherein when the first switch and the third switch of one of the capacitor [[~~pair~~]]pairs, and the second switch and the third switch of another one of the capacitor [[~~pair~~]]pairs are turned on, the capacitance of the first capacitor of the one of the capacitor [[~~pair~~]]pairs, the capacitance of the second capacitor of the another one of the capacitor [[~~pair~~]]pairs, or a ratio of a difference between the capacitance of the first capacitor of the one of the capacitor [[~~pair~~]]pairs and the capacitance of the second capacitor of the another one of the capacitor [[~~pair~~]]pairs to an average of the capacitance of the first capacitor of the one of the capacitor [[~~pair~~]] pairs and the capacitance of the second capacitor of the another one of the capacitor [[~~pair~~]]pairs is measured via the first pad, the second pad, the third pad and the fourth pad.

12. (original) The circuit of claim 9, further comprising:

a selection circuit, connected to all of the first switches, the second switches and the third switch to selectively turn on or turn off the first switches, the second switches or the third switches.

13. (original) The circuit of claim 12, further comprising a step of automatically operating the circuit via the selection circuit.

14. (original) The circuit of claim 12, the selection circuit comprises a shift register.